FIG. 1

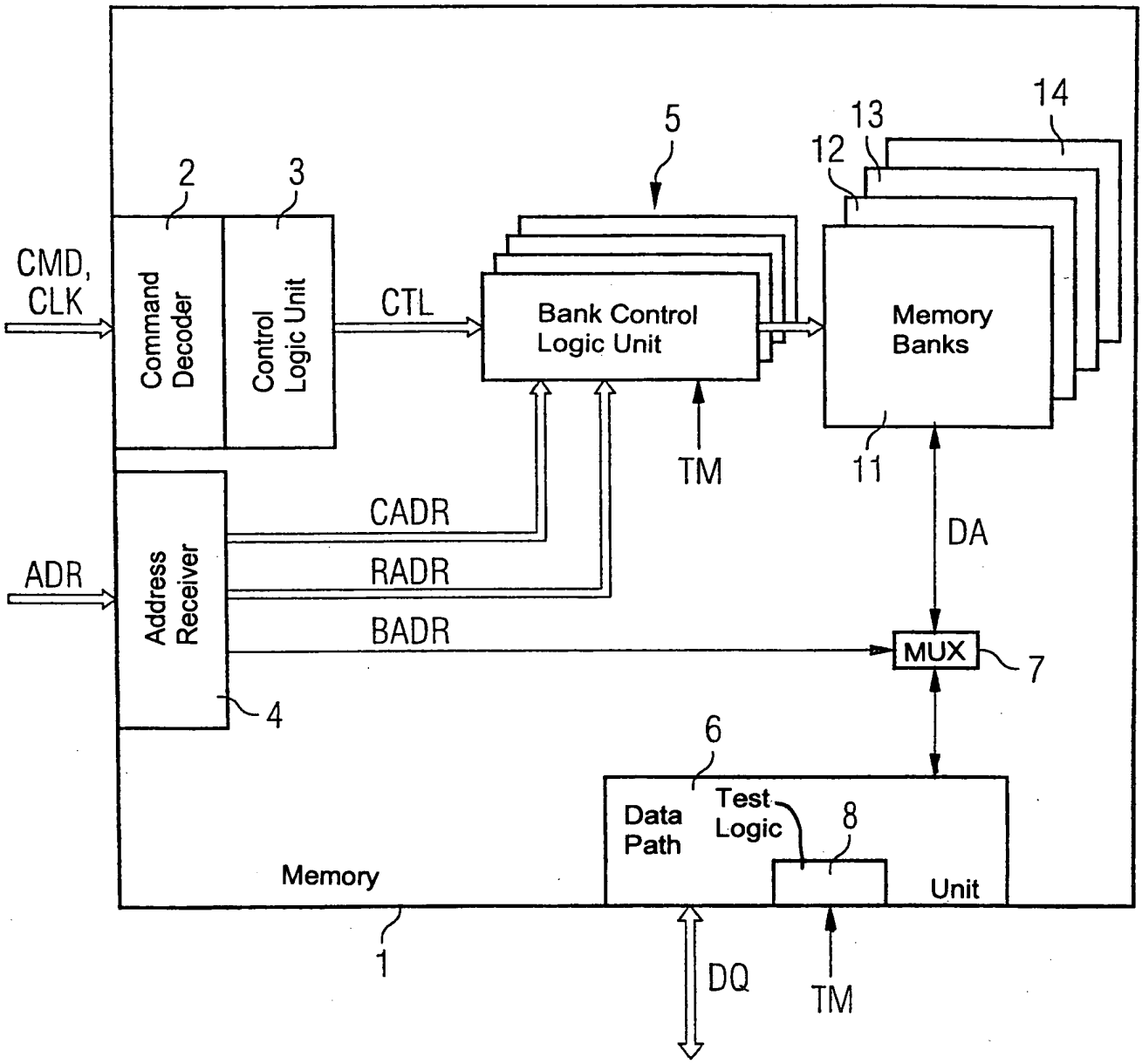
CMD,
CLK
Command Decoder
Control Logic Unit
CTL
Bank Control Logic Unit
Memory Banks
2
3
5
12
13
14
TM
11
DA
ADR
Address Receiver
CADR
RADR
BADR
MUX
7
4
6
Data Path
Test Logic
8
Unit
Memory
1
DQ
TM

FIG. 2

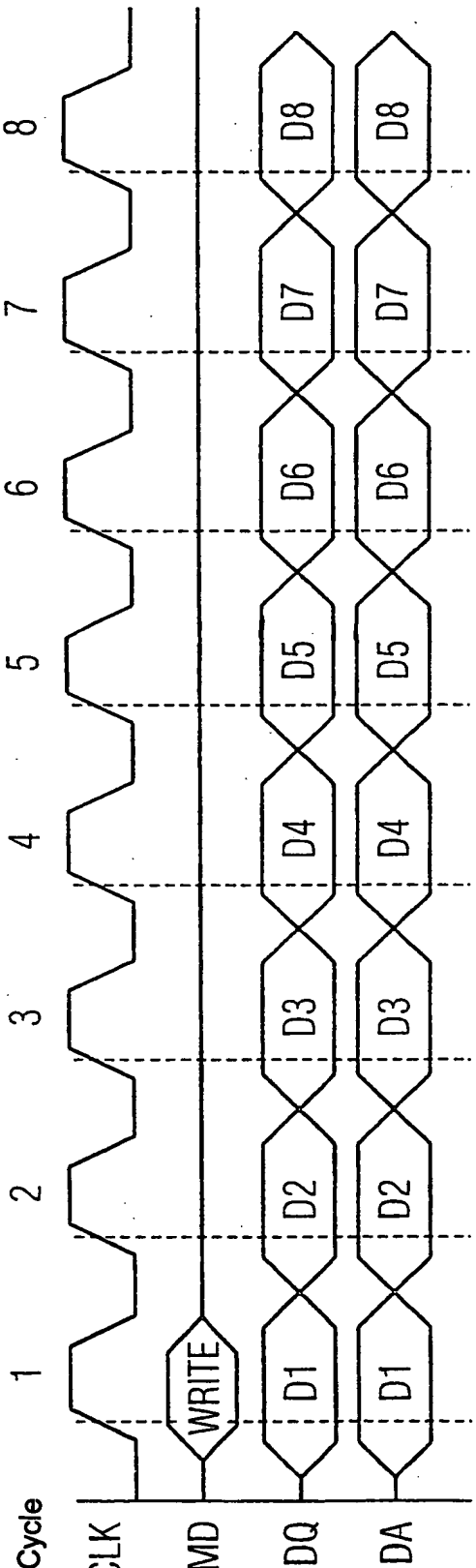
Clock Cycle
1
2
3
4
5
6
7
8
CLK
CMD
DQ
DA
WRITE
D1
D2
D3
D4
D5
D6
D7
D8

FIG. 3

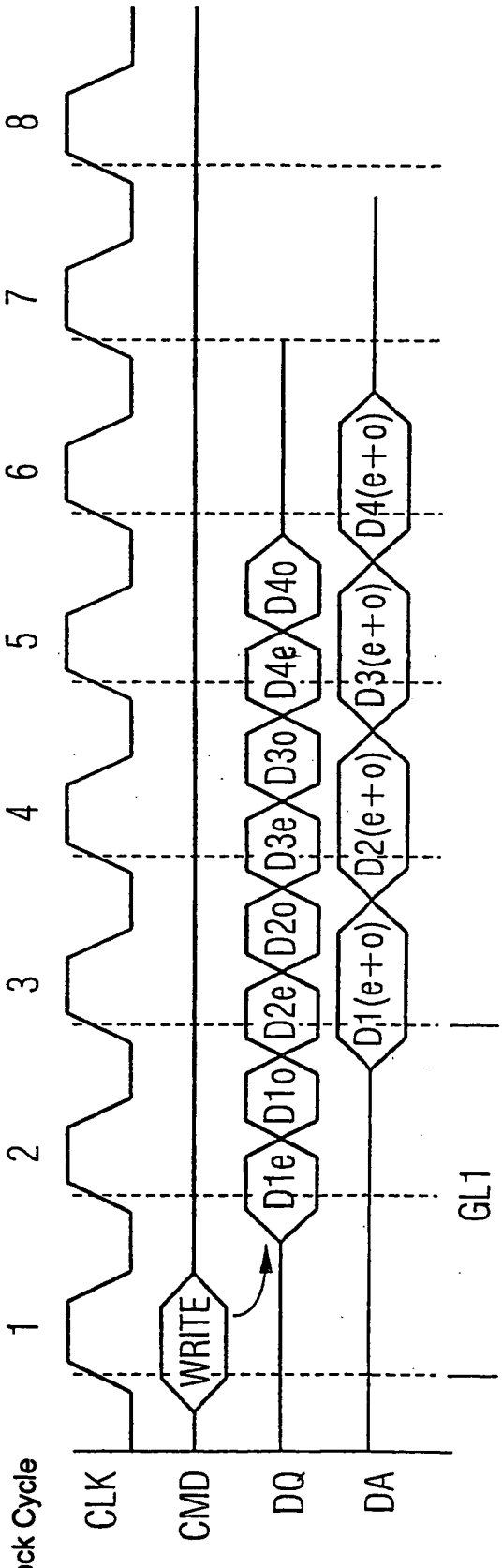
Clock Cycle
1
2
3
4
5
6
7
8
CLK
CMD
DQ
DA
WRITE
D1e
D1o
D2e
D2o
D3e
D3o
D4e
D4o
D1(e+o)
D2(e+o)
D3(e+o)
D4(e+o)
GL1

FIG. 4

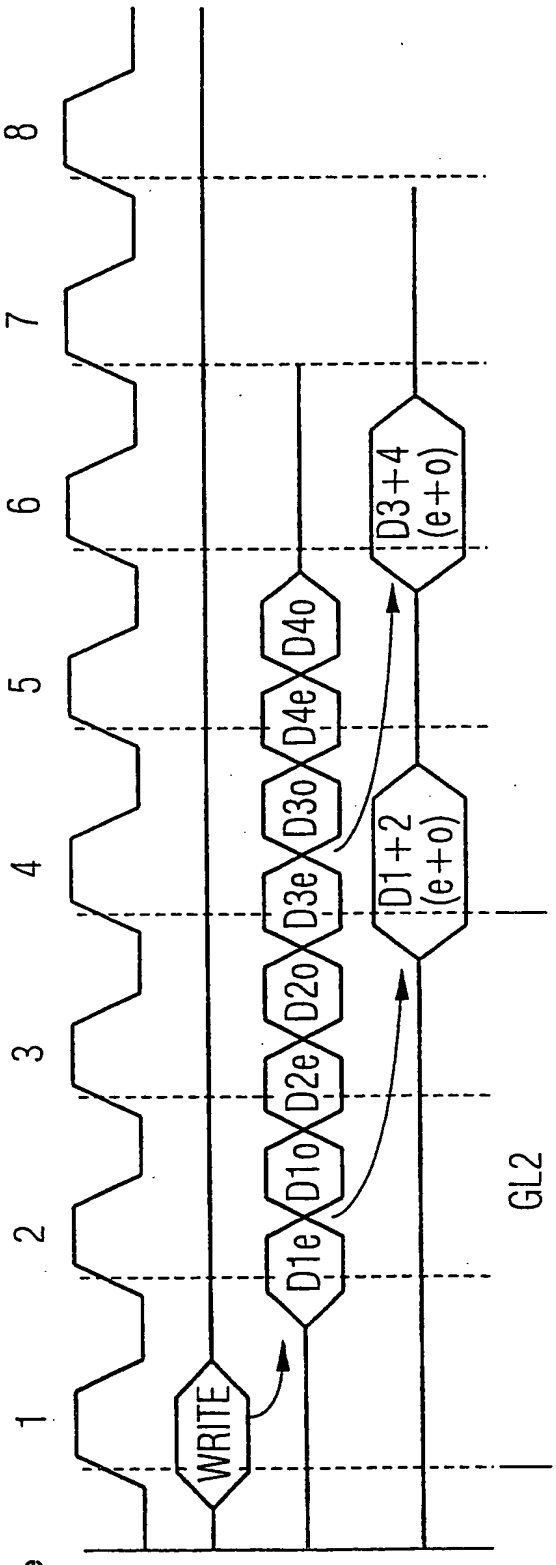
Clock Cycle
1
2
3
4
5
6
7
8
CLK
CMD
DQ
DA
WRITE
D1e
D1o
D2e
D2o
D3e
D3o
D4e
D4o
D1+2 (e+o)
D3+4 (e+o)
GL2

FIG. 5

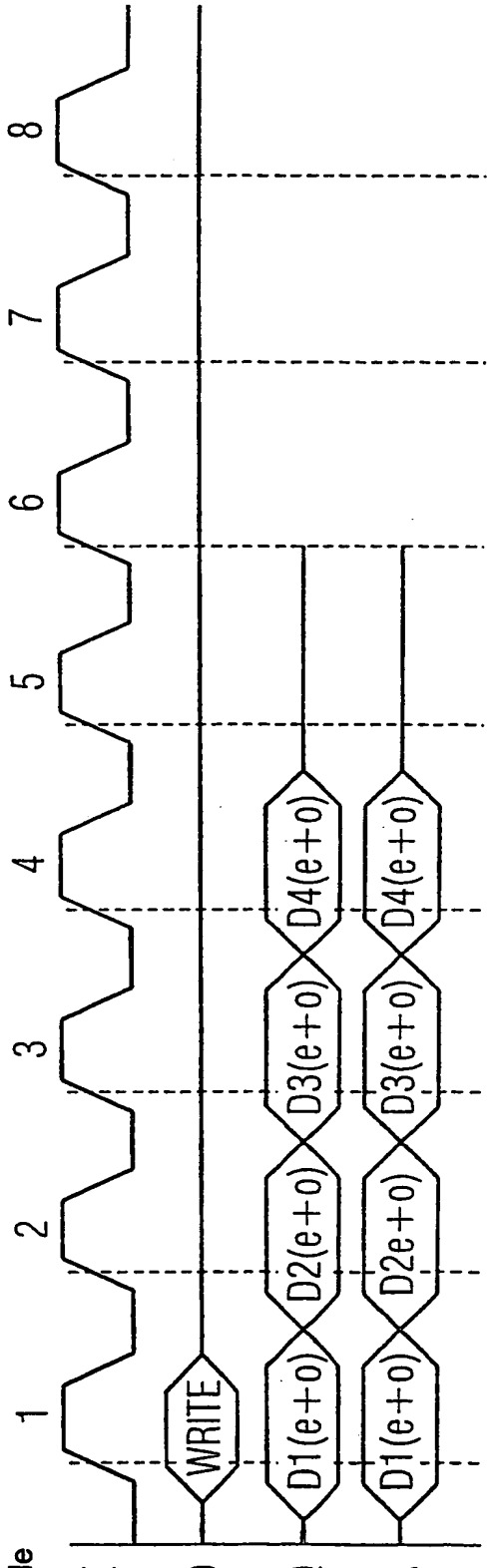
Clock Cycle
1
2
3
4
5
6
7
8
CLK
CMD
DQ
DA
WRITE
D1(e+o)
D2(e+o)
D3(e+o)
D4(e+o)
D1(e+o)
D2e+o)
D3(e+o)
D4(e+o)

FIG. 6

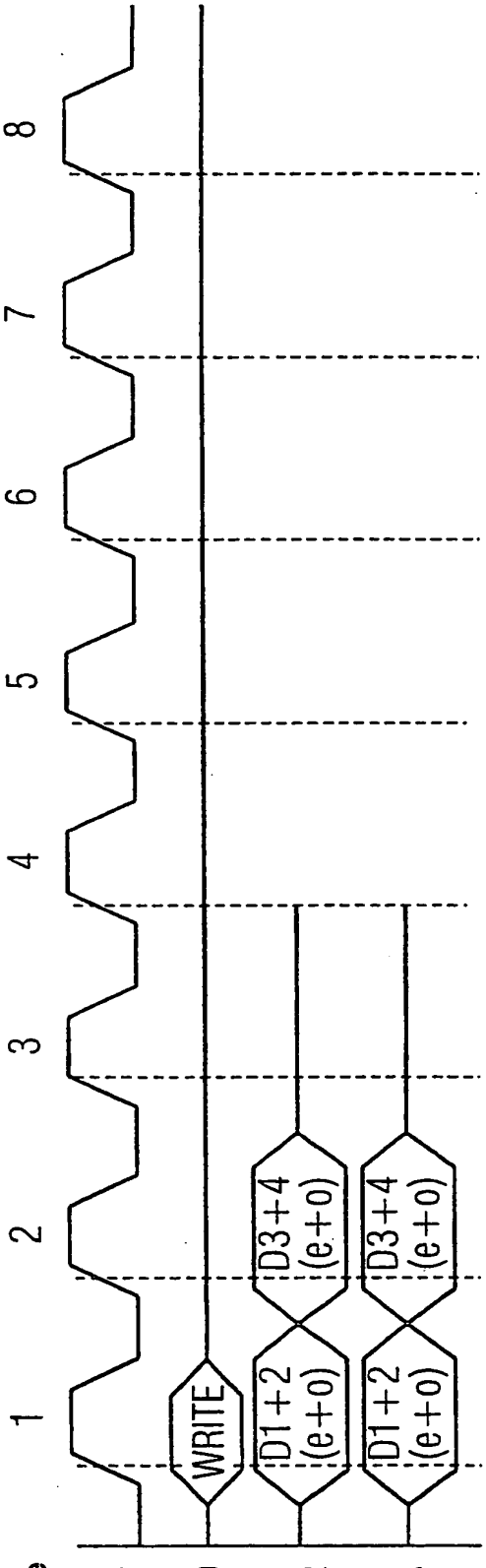
Clock Cycle
1
2
3
4
5
6
7
8
CLK
CMD
DQ
DA
WRITE
D1+2 (e+o)
D3+4 (e+o)
D1+2 (e+o)
D3+4 (e+o)

FIG. 7

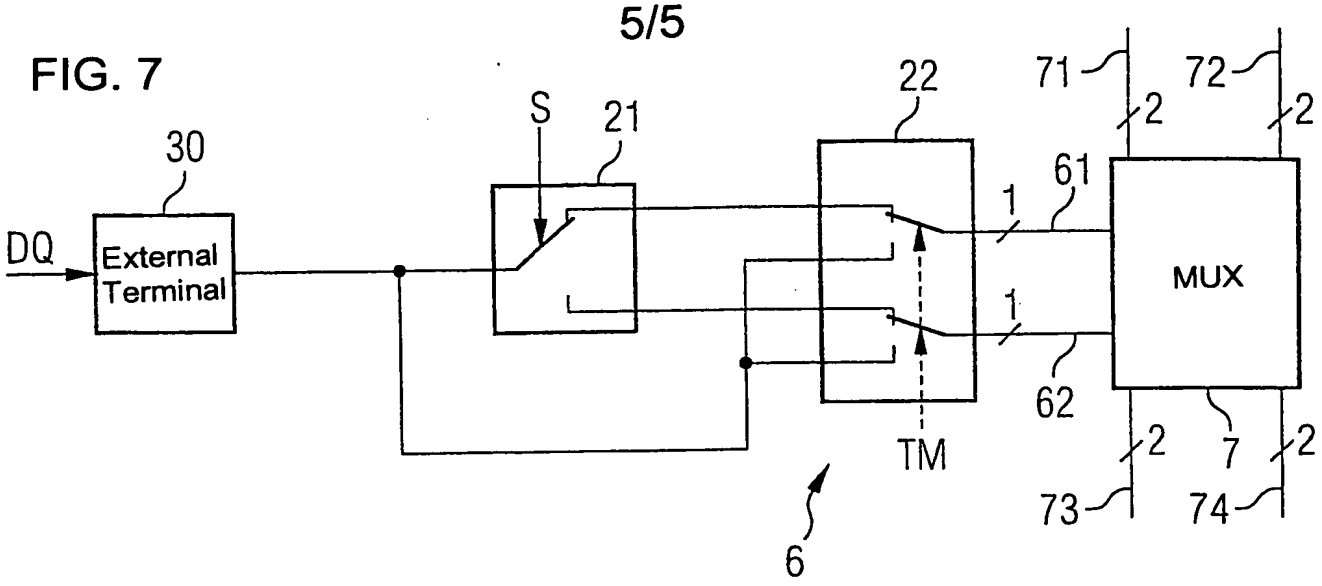

FIG. 8

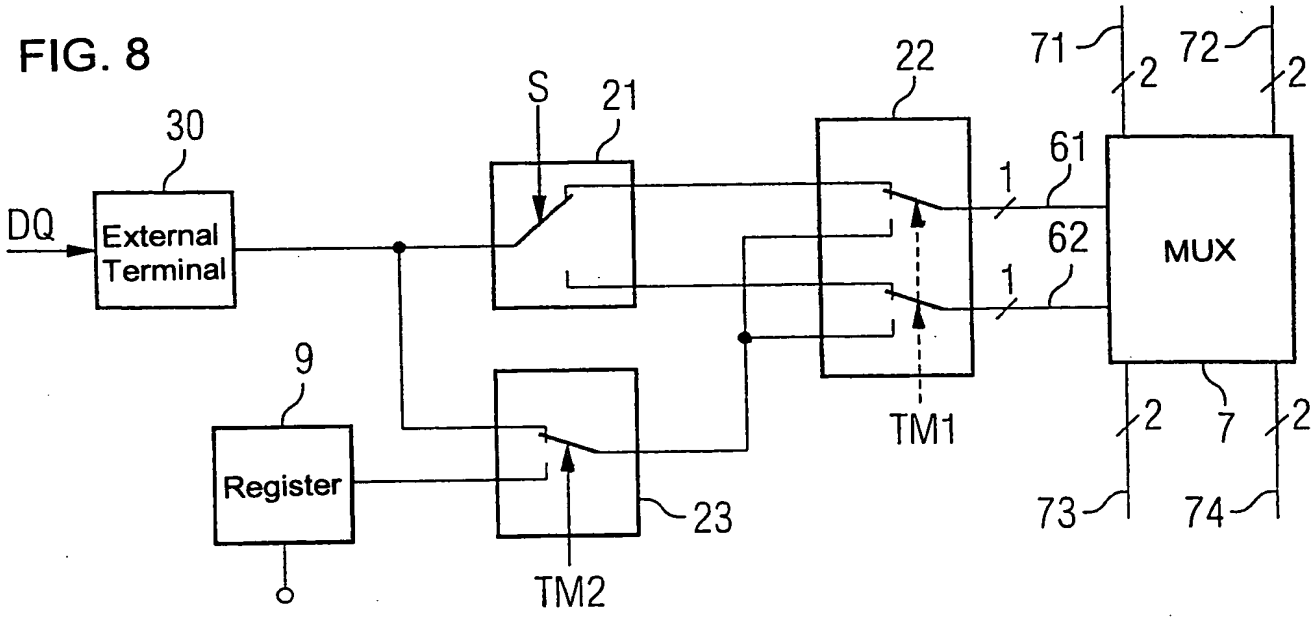
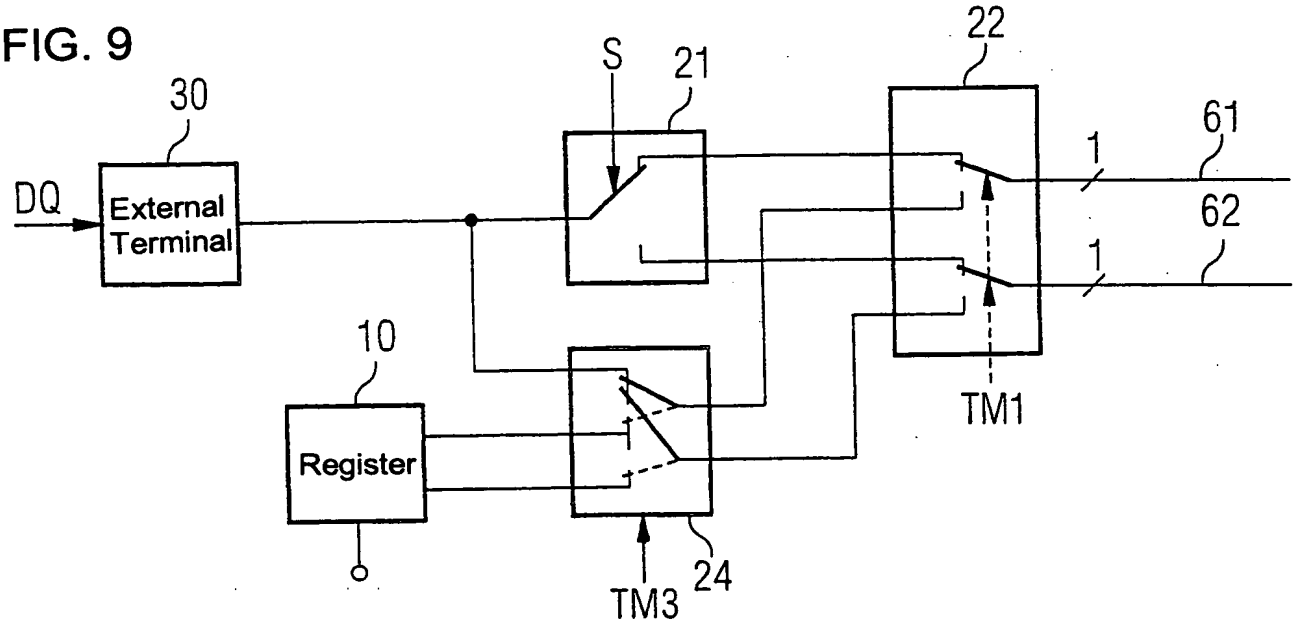
FIG. 9